Remarks:

Reconsideration of the application is requested.

Claims 1-13 remain in the application. Claims 1-13 are subject to examination. Claims 1 and 9 have been amended.

In item 4 on page 4 of the above-identified Office action, the Examiner objected to claim 1 because of an informality. Claim 1 has been amended with the words "configured for" as suggested by the Examiner.

In items 5 and 6 on pages 4 and 5 of the above-identified Office action, claims 1 and 9 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that the recitation of "said processing device" in claim 1 does not have sufficient antecedent basis. The words "processing device" have been changed to "processing unit".

In regards to claim 9, the Examiner asks how there can be a plurality of test data items to be compared with each other. Claim 9 has been amended to delete the wording "plurality of".

It is further noted that the Examiner states that the steps in claim 9 must be indented. Please note that MPEP 608.01(m) uses the terminology may be indented. As noted by the Examiner, indentations are used for segregating substeps. There are no substeps recited in claim 9, they are the main steps. Should the Examiner still disagree a quick discussion with the Examiner's mentor or supervisor will quickly clear up this issue as the undersigned has prosecuted thousands of patents without ever running into this rejection.

It is accordingly believed that claims 1 and 9 meet the requirements of 35 U.S.C. § 112, second paragraph. The above noted changes to the claims are provided solely for the purpose of satisfying the requirements of 35 U.S.C. § 112. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In the above-identified Office action, claims 1-13 have been rejected as being obvious over U.S. Patent No. 6,085,346 to Lepejian et al. (hereinafter Lepejian) in view of U.S. Patent No. 6,691,271 to Kanehira et al. (hereinafter Kanehira) under 35 U.S.C. § 103.

The invention of the instant application as recited in claim 1, relates to a circuit for testing a data memory. A

processing unit applies a first function to a predetermined test pattern for generating data items therefrom and for applying a second function to some of the data items read from the data memory for generating test data items therefrom. The first and second functions are defined and provided by the processing unit. The comparison device compares then compares the test data items generated by the second function with each other and with the predetermined test pattern upon which the first function was not performed.

In view of the Examiner's statement that claim 1 does not recite comparing any of the test data items with each other, applicant has amended claims 1 and 9 to make it clear that the data items are compared with each other and/or with the predetermined test pattern. Support for the changes to claims 1 and 9 is found on page 14, lines 6-19 of the specification of the instant application.

Lepejian discloses a BIST circuit. The difference between the BIST circuit according to Lepejian and the invention of the instant application is that the invention of the instant application is not limited to only comparing data written into and read out of the data memory but compares the data before the first function is applied to the test pattern data and with the resulting data after the second function is applied. In other words, Lepejian teaches a comparison between the data

written into and read out of the memory while the invention of the instant application teaches to compare encoded data, i.e. data before the operation with the first function and after the operation of the second function. Thereby, the overall number of comparisons needed to detect a memory error can be substantially reduced. This is because the data items resulting from the second function and the predetermined data pattern all should be the same and can be compared with each other rather than outside data.

The Examiner states that Lepejian does not teach the application of a second function to the data items read form the data memory for generating thereform test data items and relies on Kanehira to teach a second function.

Kanehira teaches a BIST circuit for testing integrated circuits. What is not disclosed is a BIST circuit for testing a data memory. Kanehira discloses the application of a first function and a second function on data patterns provided by a signal generator. Referring to Fig. 8, the first function is formed in block 7 and the second function is performed in block 9. The two blocks 7, 9 are connected in series and no further operation is carried out using the data provided at the output of block 7 (between the two blocks). Furthermore, we could not find any suggestion that the data output by the block 7 providing the first function is written into a data

memory or is forwarded to any other operation than the block 9 for providing the second function. Kanehira relates to a self test method for testing the correct functioning of the block 9 by applying data which are a result of a reciprocal function to the function of block 9. A person of average skill in the art is neither incited nor motivated to take Kanehira into account, as no hint is given therein to write the data output by block 7 to a data memory or - to put it simply - to use the BIST method for testing a memory device.

Furthermore, if a person of average skill in the art combined the teachings of Lepejian and Kanehira, he or she would come to a circuit wherein either the data written into the data memory is generated by applying both the first and the second function in the blocks 7 and 9, or the data read out of the data memory is processed with both the first and second function as performed in the blocks 7 and 9. This would not lead to the result that the data comparison is performed with encoded data (the data item before the first function is applied and data items after the second function is applied) with a number of the test data items being smaller than the number of data items provided to the data memory (e.g. not all of the data read from the memory has the second function applied to it). Thus, we cannot see how a person of average skill in the art is incited or motivated to combine the documents as he or she would not obtain an advantage

therefrom.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 9. Claims 1 and 9 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 9.

In view of the foregoing, reconsideration and allowance of claims 1-13 are solicited.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

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REL:kf

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